AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) A method for use in connection with an integrated circuit design, the method comprising:

determining timing differences for respective ones of a plurality of paths, an individual timing difference being between an individual path of the plurality of paths including a low threshold variant of a gate instance and the individual path including a standard threshold variant of the gate instance, the individual path including at least one low threshold variant of a gate instance;

determining a first set of path cycle times for respective ones of at least a subset of the plurality of paths, the subset corresponding to individual paths of the plurality of paths, the individual paths including a particular low threshold variant of a gate instance, a timing difference corresponding to at least one of the individual paths of the subset being a slowdown;

determining a second set of path cycle times for respective ones of the subset of the plurality of paths, the individual paths including a standard threshold variant corresponding to the particular low threshold variant, thereby removing the timing difference from the individual paths;

selecting a subset of low threshold voltage variants of gate instances for substitution with respective standard threshold voltage variants thereof based on at least a maximum of the first set of path cycle times and a maximum of the second set of path cycle times for a corresponding low threshold voltage variant.

2. (Canceled)

3. (Currently amended) The method of claim ~~2~~ 1, wherein the ~~measurement includes~~ timing difference is based on at least an input slew rate of ~~each~~ an individual gate instance in ~~a~~ at least one individual circuit path.

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4. (Currently amended) The method of claim 3, wherein the input slew rate is based at least in part on a̲ falling edge input t̶r̶a̶n̶s̶i̶t̶i̶o̶n̶s̶ transition.

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently amended) The method of claim 2̶ 1̲, wherein the timing p̶e̶n̶a̶l̶t̶y̶ difference exceeds a threshold.

12. (Original) The method of claim 1, further comprising substituting in the integrated circuit design, the selected low threshold voltage variants with the respective standard threshold voltage variants thereof.

13. (Original) The method of claim 12, further comprising fabricating an integrated circuit including the substituted standard threshold voltage gate instances.

14. (Original) The method of claim 1, further comprising preparing the integrated circuit design and thereafter performing the selecting for substitution.

15. (Currently amended) A semiconductor integrated circuit comprising:
a plurality of gate instances;
circuit paths defined through respective ones of the gate instances;
wherein a subset of the gate instances are standard threshold voltage variants substituted
in the semiconductor integrated circuit based on a̶ m̶e̶a̶s̶u̶r̶e̶m̶e̶n̶t̶ i̶n̶d̶i̶c̶a̶t̶i̶n̶g̶ a̶ l̶o̶w̶

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~~threshold voltage variant penalty for the circuit paths including the subset of the gate instances~~ at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant;

wherein the first set of path cycle times are determined for respective ones of at least a subset of a plurality of the circuit paths, the subset corresponding to individual paths of the plurality of the circuit paths, the individual paths including a particular low threshold variant of a gate instance, a timing difference corresponding to at least one of the individual paths of the subset being a slowdown;

wherein the second set of path cycle times are determined for respective ones of the subset of the plurality of the circuit paths, the individual paths including a standard threshold variant corresponding to the particular low threshold variant, thereby removing the timing difference from the individual paths;

wherein the timing differences corresponding to respective ones of the plurality of the circuit paths, an individual timing difference being between an individual path of the plurality of the circuit paths including a low threshold variant of a gate instance and the individual path including a standard threshold variant of the gate instance, the individual path including at least one low threshold variant of a gate instance.

16. (Currently amended) The semiconductor integrated circuit of claim 15, wherein the ~~measurement includes~~ timing difference is based on at least an input slew ~~rates~~ rate for at least one gate ~~instances~~ instance in ~~the~~ at least one individual circuit ~~paths~~ path ~~including the subset of the gate instances~~.

17. (Currently amended) The semiconductor integrated circuit of claim 16, wherein the input slew rate is based at least in part on a falling edge input ~~transitions~~ transition.

18. (Currently amended) A computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding comprising:

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one or more design file media encoding representations of a plurality of gate instances; and

one or more design file media encoding representations of circuit paths defined through respective ones of the gate instances,

wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on ~~a measurement indicating a low threshold voltage variant timing penalty~~ at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant;

wherein the first set of path cycle times are determined for respective ones of at least a subset of a plurality of the circuit paths, the subset corresponding to individual paths of the plurality of the circuit paths, the individual paths including a particular low threshold variant of a gate instance, a timing difference corresponding to at least one of the individual paths of the subset being a slowdown;

wherein the second set of path cycle times are determined for respective ones of the subset of the plurality of the circuit paths, the individual paths including a standard threshold variant corresponding to the particular low threshold variant, thereby removing the timing difference from the individual paths;

wherein the timing differences corresponding to respective ones of the plurality of the circuit paths, an individual timing difference being between an individual path of the plurality of the circuit paths including a low threshold variant of a gate instance and the individual path including a standard threshold variant of the gate instance, the individual path including at least one low threshold variant of a gate instance.

19. (Currently amended) The computer readable encoding of a semiconductor integrated circuit design of claim 18, wherein the ~~measurement includes~~ timing difference is based on at least an input slew ~~rates~~ rate for at least one gate ~~instances~~ instance in ~~the circuit paths including the subset of the gate instances~~ at least one individual circuit path.

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20. (Currently amended) A method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit, the method comprising:

preparing the one or more design files for the semiconductor integrated circuit including at least one low threshold voltage instance and performing timing analysis thereon;

substituting at least one of the low threshold voltage instances of the semiconductor integrated circuit with a standard threshold voltage instance; and

generating one or more design file outputs that encode representations of the semiconductor integrated circuit, including the substituted standard threshold voltage instances; and

supplying the one or more design file outputs as at least part of the computer readable media product;

wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant;

wherein the first set of path cycle times are determined for respective ones of at least a subset of a plurality of paths, the subset corresponding to individual paths of the plurality of paths, the individual paths including a particular low threshold variant of a gate instance, a timing difference corresponding to at least one of the individual paths of the subset being a slowdown;

wherein the second set of path cycle times are determined for respective ones of the subset of the plurality of paths, the individual paths including a standard threshold variant corresponding to the particular low threshold variant, thereby removing the timing difference from the individual paths;

wherein the timing differences corresponding to respective ones of the plurality of paths, an individual timing difference being between an individual path of the plurality of paths including a low threshold variant of a gate instance and the individual path including a standard threshold variant of the gate instance, the individual path including at least one low threshold variant of a gate instance.

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21. (Cancelled)

22. (Currently amended) The method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit of claim 20, wherein the substituting is based at least in part on a measurement including an input slew rates rate for at least one gate instances instance in the circuit paths including the subset of the gate instances.

23. (Currently amended) An apparatus comprising:

means for processing one or more design files for a semiconductor integrated circuit, the one or more design files encoding representations of a plurality of gate instances and circuit paths;

means for selecting at least one of the gate instances based on a measurement that indicates a low threshold voltage variant timing penalty; and

means for substituting at least one of the low threshold voltage gate instance representations with respective standard threshold voltage variants thereof;

wherein the at least one of the low threshold voltage gate instance representations is selected based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant;

wherein the first set of path cycle times are determined for respective ones of at least a subset of a plurality of paths, the subset corresponding to individual paths of the plurality of paths, the individual paths including a particular low threshold variant of a gate instance, a timing difference corresponding to at least one of the individual paths of the subset being a slowdown;

wherein the second set of path cycle times are determined for respective ones of the subset of the plurality of paths, the individual paths including a standard threshold variant corresponding to the particular low threshold variant, thereby removing the timing difference from the path;

wherein the timing differences corresponding to respective ones of the plurality of paths, an individual timing difference being between an individual path of the plurality of paths including a low threshold variant of a gate instance and the individual

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path including standard threshold variant of the gate instance, the individual path including at least one low threshold variant of a gate instance.

24. (New) The semiconductor integrated circuit of claim 15, wherein the timing difference exceeds a threshold.

25. (New) The computer readable encoding of a semiconductor integrated circuit design of claim 19, wherein the input slew rate is based at least in part on a falling edge input transition.

26. (New) The computer readable encoding of a semiconductor integrated circuit design of claim 18, wherein the timing difference exceeds a threshold.

27. (New) The method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit of claim 22, wherein the input slew rate is based at least in part on a falling edge input transition.

28. (New) The method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit of claim 20, wherein the timing difference exceeds a threshold.

29. (New) The apparatus of claim 23, wherein the timing difference is based on at least an input slew rate of an individual gate instance.

30. (New) The apparatus of claim 29, wherein the input slew rate is based at least in part on a falling edge input transition.

31. (New) The apparatus of claim 29, wherein the timing difference exceeds a threshold.

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